Fault attacks on two software countermeasures

Nicolas Moro\textsuperscript{*,1}, Karine Heydemann\textsuperscript{†}, Amine Dehbaoui\textsuperscript{‡}, Bruno Robisson\textsuperscript{*}, Emmanuelle Encrenaz\textsuperscript{†}

\textsuperscript{*}Commissariat à l’Énergie Atomique et aux Énergies Alternatives (CEA), F-13541 Gardanne, France - nicolas.moro@cea.fr
\textsuperscript{†}Sorbonne Universités, UPMC Univ Paris 06, UMR 7606, LIP6, F-75005 Paris, France - karine.heydemann@lip6.fr
\textsuperscript{‡}SERMA Technologies, CESTI, F-33615 Pessac, France - a.dehbaoui@serma.com

Abstract—Injection of transient faults can be used as a way to attack embedded systems. On embedded processors such as microcontrollers, several studies showed that such a transient fault injection could corrupt either the data loads from the memory or the assembly instructions executed by the circuit. Some countermeasure schemes which rely on temporal redundancy have been proposed to handle this issue. Among them, several schemes add this redundancy at assembly instruction level. In this paper, we perform a practical evaluation for two of those countermeasure schemes by using a pulsed electromagnetic fault injection process on a 32-bit microcontroller.

I. INTRODUCTION

In this paper, we experimentally evaluate the robustness of two software countermeasure schemes against fault injection on embedded programs. Both countermeasures are designed at assembly code level and rely on providing some replacement sequences to strengthen some sensitive instructions. To perform this evaluation, we use a pulsed electromagnetic fault injection technique. This fault injection technique has turned out to be an effective way to inject transient faults in a circuit’s computation [3]. Figure 1 shows an architectural view of the electromagnetic fault injection platform used in this paper. It is similar to the one presented in [4].

![Electromagnetic fault injection bench](image)

The chosen target is an up-to-date 32-bit microcontroller designed in a CMOS 130 nm technology based on the ARM Cortex-M3 processor [5]. Its operating frequency is set to 56 MHz without any cache memory, and no prefetch buffer is activated. Cortex-M3 processors use a Harvard architecture and run the ARM Thumb-2 instruction set [6], which contains both 16-bit and 32-bit instructions. Some 16-bit instructions can be forced to a 32-bit encoding by using a specific syntax.

II. EVALUATION OF THE COUNTERMEASURES

A. Evaluation approach

We need to define a relevant metric to evaluate the efficiency of the countermeasures. Since the countermeasure sequences add some instructions, the time to execute a full countermeasure sequence becomes longer than the time to execute the initial instruction. Thus, the number of vulnerable points, \textit{i.e.} the injection times for which a fault injection attempt is successful, may also increase. Comparing the percentage of faulty outputs could appear to be a solution to compare two data sets with different numbers of measurements. Nevertheless, we assume that the most meaningful metric for such a comparison is the number of faults that have been obtained on the destination register. The countermeasure is really effective if it can overcome the fact that some new vulnerable points are added and if it can decrease this number of vulnerable points. Thus, comparing the number of faulty outputs is probably the most relevant metric for an attacker since it indicates the number of potential vulnerabilities on an embedded code.

B. Fault tolerance countermeasure

This countermeasure aims at providing a fault-tolerant replacement sequence for most of the instruction of an instruction set [1]. Such a countermeasure has been designed to be tolerant to any single instruction skip and does not provide any protection to the data flow. An example of the use of this countermeasure is given in Listing 1.

Listing 1. Fault detection countermeasure for a \texttt{bl <function>} instruction

\begin{verbatim}
1: \textbf{adr} \texttt{r1, <return_label>}
2: \textbf{adr} \texttt{r1, <return_label>}
3: \textbf{add} \texttt{lr, r1, #1} 7 Thumb mode requires the
4: \texttt{add} \texttt{lr, r1, #1} ; last bit of LR to be set
5: \texttt{b <function>}
6: \texttt{b <function>}
7: \texttt{return_label:}
\end{verbatim}

We performed some fault injection experiments on four codes: a \texttt{bl} instruction without countermeasure (100 ns time interval by steps of 200 ps), a \texttt{bl.w} instruction with forced 32-bit encoding without countermeasure (100 ns), the replacement sequence presented in Listing 1 (400 ns) and this replacement sequence with forced 32-bit encoding (400 ns). Several values were used for the pulse voltage, from $-210$ V to $-170$ V and from $120$ V to $150$ V by steps of 5 V. The target circuit crashes for voltages over $150$ V. In this experiment, the subroutine that is called only modifies $r0$. Thus, we analyze the number of faults in $r0$ at the end of the experiment to evaluate the efficiency of the countermeasure. The faults on any register curves correspond to an output in which at least one register contains a faulty value.

The fault injection results are shown on Fig. 2. We can observe that applying the countermeasure without forced 32-bit encoding does not seem to be efficient. Indeed, this
countermeasure has not been designed to be resistant to two consecutive instruction corruptions. Because of the memory alignment in the experiment, in the replacement sequence the first two adr instructions and later the last two b instructions are loaded in a single fetch stage. Thus, it seems that such double corruption happened. Moreover, we can also observe that no faulty output has been obtained for pulses with a negative voltage on a single 32-bit b1.w instruction. Nevertheless, such an instruction could still be faulted by using pulses with a positive voltage. An explanation for such result can be found in the way instructions are encoded. The 16-bit subset of the instruction set is very compact (most of the 16-bit values correspond to one instruction) while the 32-bit subset is very sparse: very few bit flips can change a 16-bit instruction. Thus, it seems such a sensitive instruction can be significantly reinforced against fault attacks. Since this countermeasure has been formally proven resistant to instruction skips, its main limitation appears to be due to its considered fault model which might be too simplistic. Otherwise, the fault detection countermeasure has been designed to protect a smaller set of instructions. It turns out that the level of security they add could be nullified if their implementation on a target platform is not performed in the right way. The fault tolerance countermeasure has been very effective to protect an isolated subroutine call instruction. In the right way, the fault tolerance countermeasure has been reinforced against fault attacks. Since this countermeasure has been formally proven resistant to instruction skips, its main limitation appears to be due to its considered fault model which might be too simplistic. Otherwise, the fault detection countermeasure has been designed to protect a smaller set of instructions and it has been very effective on the considered test cases.

### III. Conclusion

We have provided a first attempt of practical study of two assembly-level software countermeasure against fault injection attacks. Even if those countermeasures are theoretically secure, it turns out that the level of security they add could be nullified if their implementation on a target platform is not performed in the right way. The fault tolerance countermeasure has been very effective to protect an isolated subroutine call instruction. Thus, it seems such a sensitive instruction can be significantly reinforced against fault attacks. Since this countermeasure has been formally proven resistant to instruction skips, its main limitation appears to be due to its considered fault model which might be too simplistic. Otherwise, the fault detection countermeasure has been designed to protect a smaller set of instructions and it has been very effective on the considered test cases.

### REFERENCES


